What is claimed is:

1. A liquid crystal display having an applied horizontal electric field comprising:

a gate line;

a common line substantially parallel to the gate line;

a data line arranged to cross the gate line and the common line to define a pixel area;

a thin film transistor formed at each crossing of the gate line and the data line;

a common electrode formed in the pixel area and connected to the common line;

a pixel electrode connected to the thin film transistor, wherein the horizontal electric field is formed between the pixel electrode and the common electrode in the pixel area;

a gate pad formed with at least one conductive layer included in the gate line;

a data pad formed with at least one conductive layer included in the data line;

a common pad formed with at least one conductive layer included in the common line;

a passivation film to expose at least one of the gate pad, the data pad and the common pad; and

a driving integrated circuit mounted on a substrate connected directly to one of the gate pad and the data pad.

2. The liquid crystal display according to claim 1, wherein the driving integrated circuit includes a gate driving integrated circuit connected to the gate pad.

3. The liquid crystal display according to claim 2, wherein the driving integrated circuit further includes a data driving integrated circuit connected directly to the data pad.

4. The liquid crystal display according to claim 2, wherein the driving integrated circuit further includes a data driving integrated circuit connected to the data pad using a conductive film.

5. The liquid crystal display according to claim 1, further comprising a signal supplying line for supplying a driving signal to the driving integrated circuit.

6. The liquid crystal display according to claim 1, wherein each of the gate line and the common line includes a main conductive layer and a secondary conductive layer to protect against an opening of the main conductive layer.

7. The liquid crystal display according to claim 6, wherein each of the gate pad and the common pad comprise the main conductive layer and the secondary conductive layer, and wherein the secondary conductive layer has an exposed structure.

8. The liquid crystal display according to claim 6, wherein each of the gate pad and the common pad comprises the secondary conductive layer.

9. The liquid crystal display according to claim 6, wherein the main conductive layer includes at least one of an aluminum system metal, a copper, a molybdenum, a chrome and a tungsten that are a low resistance metal,

wherein the secondary conductive layer includes a titanium.

10. The liquid crystal display according to claim 1, wherein the data pad comprises a main conductive layer and a secondary conductive layer to protect against an opening of the main conductive layer.

11. The liquid crystal display according to claim 10, wherein the secondary conductive layer has an exposed structure.

12. The liquid crystal display according to claim 10, wherein the main conductive layer includes at least one of an aluminum system metal, a copper, a molybdenum, a chrome and a

tungsten that is a low resistance metal, wherein the secondary conductive layer includes a titanium.

13. The liquid crystal display according to claim 1, the thin film transistor comprising:

a gate electrode connected to the gate line;

a source electrode connected to the data line;

a drain electrode opposite the source electrode; and

a semiconductor layer for forming a channel portion between the source electrode and the drain electrode.

14. The liquid crystal display according to claim 13, wherein the drain electrode and the pixel electrode are made of an identical conductive layer.

15. The liquid crystal display according to claim 14, wherein the semiconductor layer is formed on the gate insulating film along with the data line, the source electrode, the drain electrode and the pixel electrode.

16. A method for fabricating a liquid crystal display having a horizontal electric field comprising:

preparing a thin film transistor array substrate having a gate line and a data line, wherein a thin film transistor is formed at a crossing of the gate line and the data line, wherein the horizontal electric field is formed between a pixel electrode connected to the thin film transistor and a common electrode;

forming a conductive layer in a gate pad, a data pad, and a common pad, wherein at least one of the gate pad, data pad and common pad is exposed through a passivation film; and

mounting a driving integrated circuit on the substrate, wherein at least one of the exposed gate pad and the data pad is directly connected to the driving integrated circuit.

17. The method according to claim 16, wherein mounting the driving integrated circuit on the substrate includes directly connecting the gate pad to the driving integrated circuit.

18. The method according to claim 17, further including directly connecting the data pad to the driving integrated circuit.

19. The method according to claim 17, wherein mounting the driving integrated circuit on the substrate further includes connecting the data pad with the data driving integrated circuit using a conductive film.

20. The method according to claim 16, wherein preparing the thin film transistor substrate includes:

forming, on the substrate, a first conductive pattern group including the gate line, a gate electrode connected to the gate line, the common line substantially in parallel to the gate line, the common electrode, the gate pad and the common pad;

forming a gate insulating film on the substrate having the first conductive pattern group thereon;

forming a semiconductor layer at a predetermined area of the gate insulating film and a second conductive pattern group having the date line, a source electrode of the thin film transistor connected with the data line, a drain electrode of the thin film transistor being opposite to the source electrode, a pixel electrode connected to the drain electrode and substantially parallel to the common electrode and the data line; and

forming a passivation film to expose the gate pad, the data pad and the common pad on the gate insulation film having the second conductive pattern group and the semiconductor layer formed thereon.

21. The method according to claim 20, wherein the first conductive pattern group is formed to have a double-layer structure including a main conductive layer and a secondary conductive layer to protect against an opening of the main conductive layer.

22. The method according to claim 21, wherein forming the passivation film includes exposing the secondary conductive layer of the gate pad and the common pad.

23. The method according to claim 21, wherein forming the passivation film includes forming a contact hole that passes through the passivation film and the gate insulating film to expose the secondary conductive layer.

24. The method according to claim 21, wherein the forming the passivation film includes forming a contact hole that passes through the passivation film, the gate insulation film and the main conductive layer to expose the secondary conductive layer.

25. The method according to claim 21, wherein the main layer includes at least one of an aluminum system metal, a copper, a molybdenum, a chrome and a tungsten which is a low resistance metal, and wherein the secondary conductive layer includes a titanium.

26. The method according to claim 20, wherein the second conductive pattern group is formed to have a double-layer structure including a main conductive layer and a secondary conductive layer to protect against the opening of the main conductive layer.

27. The method according to claim 26, wherein forming the passivation film includes exposing the secondary conductive layer of the data pad.

28. The method according to claim 26, wherein forming the passivation film includes forming a contact hole that passes through the passivation film to expose the secondary conductive layer.

29. The method according to claim 26, wherein forming the passivation film includes forming a contact hole that passes through the passivation film and the main conductive layer of the data pad to expose the secondary conductive layer.

30. The method according to claim 26, wherein the main conductive layer includes at least one of an aluminum system metal, a copper, a molybdenum, a chrome and a tungsten which is a low resistance metal, and wherein the secondary conductive layer includes a titanium.